IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | Leonard Forbes | Examiner: Mark V. Prenty |
| Serial No.: | 09/132,157 | Group Art Unit: 2822 |
| Filed: | August 11, 1998 | Docket: 303.229US2 |
| Title: | SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH | |

#18 Declaration 7/11/00

## DECLARATION OF INVENTOR UNDER 37 C.F.R. §1.132

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231



Sir:

I, Leonard Forbes, declare and say as follows:

1. I am the sole inventor of the subject matter claimed in the above-identified U.S. patent application Serial No. 09/132,157.

2. I am employed as a consultant for Micron Technologies, Inc.

3. I submit inventions to Micron Technologies, Inc. as confidential and proprietary information.

4. As a consultant for Micron Technologies, Inc., I submitted the subject matter claimed in the above-identified U.S. patent application Serial No. 09/132,157 to Micron Technologies, Inc., under confidential and proprietary status, as part of an invention disclosure form.

5. The same subject matter was submitted under obligation according to my consultant relationship with Micron Technology, Inc. and the invention rights were assigned to Micron Technology, Inc.

6. I have read and understood the Final Office Action issued in the above-identified application dated February 2, 2000.

7. The technique described in U.S. Patent No. 5,426,069 to Selvakumar et al. is not consistent with the basic physical phenomena such as described in the article by B.S Myerson entitled *High-Speed Silicon-Germanium Electronics* published in Scientific American, pp. 62-67, March 1994. I believe that the techniques described in the Selvakumar et al. patent

will not work and are not compatible with PMOS devices.

8. The Scientific American article by B.S Myerson and his fellow IBM researchers clearly states, beginning on page 64, middle column, line 37, to page 65, middle column, line 12 (as indicated on the attached copy) that there are serious restrictions on the composition ratios of silicon and germanium, thickness of the layers, and processing temperatures which can be employed to produce defect-free transistor quality layers of SiGe. The IBM researchers clearly state that at temperatures of 1100 degrees C and 1000 degrees C the strained layers of SiGe become defective. Also, they clearly state that at temperatures above 800 degrees C the dopant atoms in silicon or germanium quickly diffuse away from their initial position.

9. In U.S. Patent No. 5,426,069, Selvakumar et al., describe at the bottom of column 3 and top of column 4 of using a gate oxidation of 1100 degrees C for 50 minutes and a 20 minute anneal to given a gate oxide thickness of 100nm(1000 Å). At these times and temperatures, the implanted germanium atoms would have diffused far away and the layers would have become relaxed and defective.

10. Likewise, U.S. Patent No. 5,296,386 to Aronowitz et al. describes in column 2, line 18 of implantation into silicon followed by a 900C for 30-60 minutes to achieve a germanium concentration of at least 95% in the layer. This patent was filed in 1991 and in light of more recent understandings, as described by IBM scientists in the above Scientific American article, this technique is just not physically possible.

11. My patent application listed above describes a technique of a strained layer with definitive limits on thickness and composition ratios involving only low temperature processing. The germanium is implanted through the gate oxide and only low temperature processing is employed after this step.

12 U. S. Patent No. 5,818,100 to Grider at al. describes PMOS devices which are consistent with the accepted scientific principles which impose limits on the thickness of layers, maximum concentration of germanium, and the requirements for low temperature processing. The layers described by Grider et al., are however all formed by epitaxial

techniques, either ultra-high vacuum CVD or MBE, not ion implantation and solid phase epitaxial regrowth at low temperatures.

13. I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

12 June 2000
Dated

Leonard Forbes

Respectfully submitted,

LEONARD FORBES

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date _____ By n/a

Daniel J. Kluth
Reg. No. 32,146

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **June ___, 2000.**

n/a
Name

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Signature